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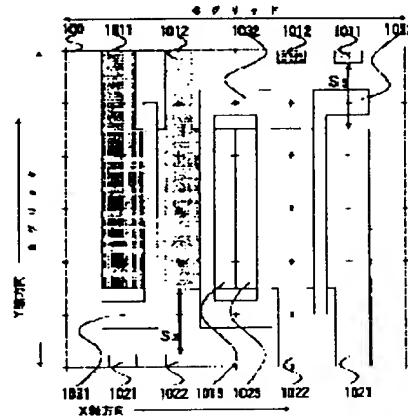
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## (54) SEMICONDUCTOR DEVICE

### (57)Abstract:

**PROBLEM TO BE SOLVED:** To reduce the area of a basic cell by forming diffused layer regions with second PMOS and first NMOS diffused layers which directly adjoin in a first layout order, and forming diffused layer regions with fourth PMOS and third NMOS diffusion layers directly adjoining a second layout order.

**SOLUTION:** A basic cell 100 comprises p+-diffused layers 1011-1013 composed of two gate polysilicon PMOSs 1031, 1032, and n+ diffused layers 1021-1023 composed of two gate polysilicon NMOSs 1031, 1033. In a first layout order, they are disposed in the order PMOS, PMOS, NMOS, and NMOS. In a second layout order, they are disposed in the order NMOS, NMOS, PMOS, and PMOS. The p+ and n+-diffused layers at the sides of the PMOS and NMOS disposed at the center are directly adjoined to form a diffused layer region. By forming the diffused layer region which directly adjoins, diffused layer area can be reduced.



## LEGAL STATUS

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